

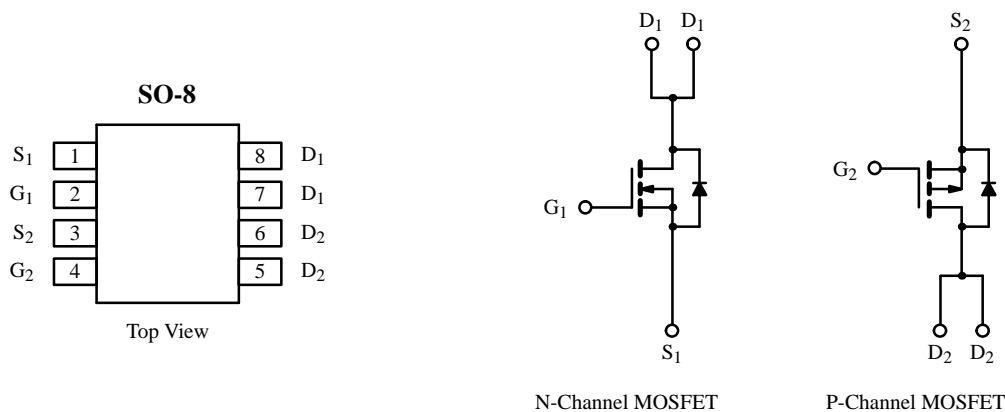
## Dual Enhancement-Mode MOSFET (N- and P-Channel)

### Product Summary

	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
N-Channel	25	0.10 @ V <sub>GS</sub> = 10 V	± 3.5
		0.15 @ V <sub>GS</sub> = 4.5 V	± 2.0
P-Channel	-25	0.25 @ V <sub>GS</sub> = -10 V	± 2.3
		0.40 @ V <sub>GS</sub> = -4.5 V	± 1.8

Recommended upgrade: Si4532DY, Si4539DY or Si9939DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6542DQ or Si6543DQ



### Absolute Maximum Ratings (T<sub>A</sub> = 25° C Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V <sub>DS</sub>	25	-25	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	± 20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	± 3.5	± 2.3
		T <sub>A</sub> = 70°C	± 2.8	± 1.9
Pulsed Drain Current	I <sub>DM</sub>	± 14	± 9.2	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	1.7	-1.6	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	2.0	
		T <sub>A</sub> = 70°C	1.3	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	62.5	°C/W

#### Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70137. A SPICE Model data sheet is available for this product (FaxBack document #70519).

## Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

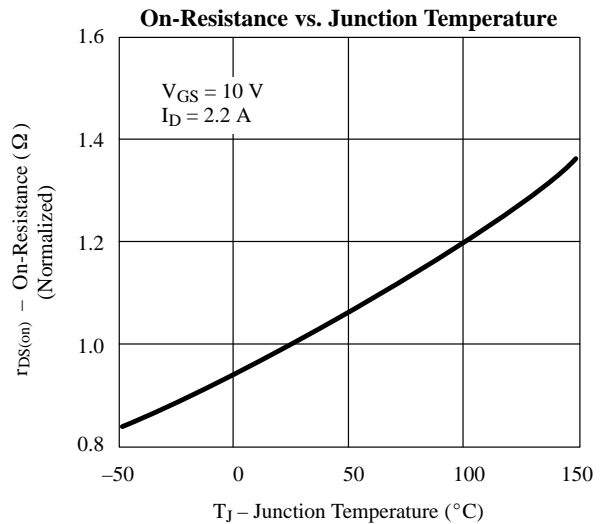
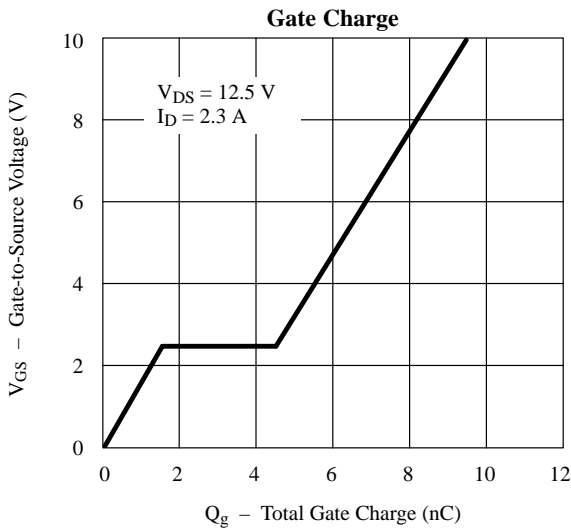
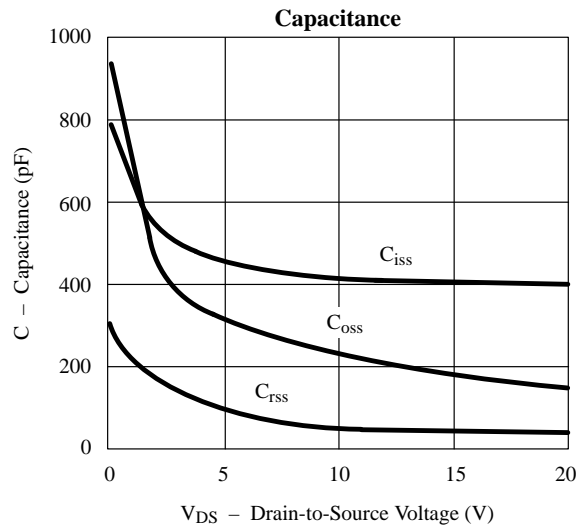
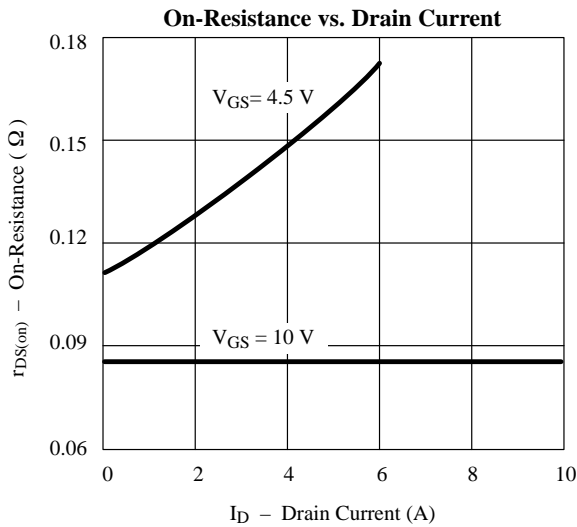
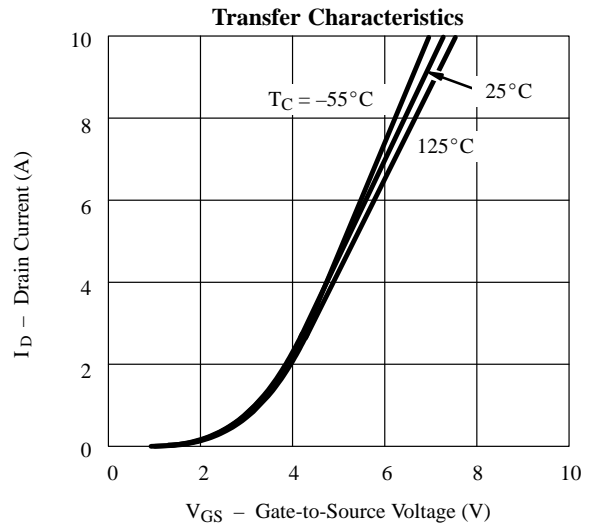
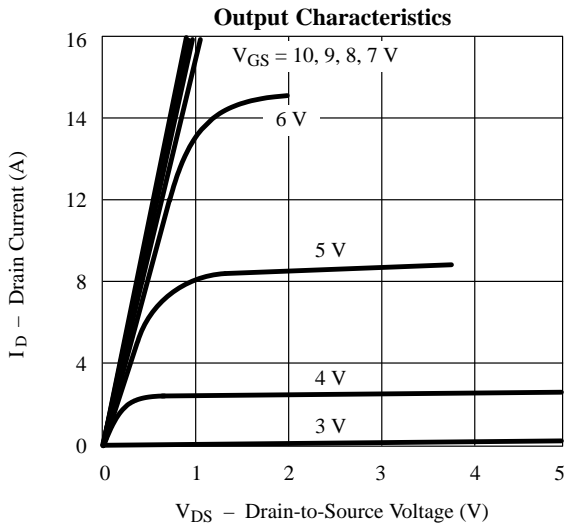
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1.0		V	
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-1.0			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch		2	$\mu\text{A}$	
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch		-2		
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$	N-Ch		25		
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$	P-Ch		-25		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch	3.5		A	
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	-2.3			
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 1 \text{ A}$	N-Ch		0.08	0.10	$\Omega$
		$V_{GS} = -10 \text{ V}, I_D = 1 \text{ A}$	P-Ch		0.13	0.25	
		$V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A}$	N-Ch		0.12	0.15	
		$V_{GS} = -4.5 \text{ V}, I_D = 0.5 \text{ A}$	P-Ch		0.20	0.40	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 3.5 \text{ A}$	N-Ch		5.0	S	
		$V_{DS} = -15 \text{ V}, I_D = -3.5 \text{ A}$	P-Ch		3.2		
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch		1.1	1.4	V
		$I_S = -1.25 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch		-1.2	-1.6	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	$Q_g$	N-Channel $V_{DS} = 12.5 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.3 \text{ A}$ P-Channel $V_{DS} = -12.5 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -2.3 \text{ A}$	N-Ch		9.4	27	nC
Gate-Source Charge	$Q_{gs}$		N-Ch		1.6		
			P-Ch		1.3		
Gate-Drain Charge	$Q_{gd}$		N-Ch		3.1		
			P-Ch		3.0		
Turn-On Delay Time	$t_{d(on)}$		N-Ch		9	20	
		P-Ch		12	40		
Rise Time	$t_r$	N-Ch		8	20	ns	
		P-Ch		19	40		
Turn-Off Delay Time	$t_{d(off)}$	N-Ch		45	90		
		P-Ch		42	90		
Fall Time	$t_f$	N-Ch		25	50		
		P-Ch		27	50		
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch				75
			P-Ch		69		100

Notes

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

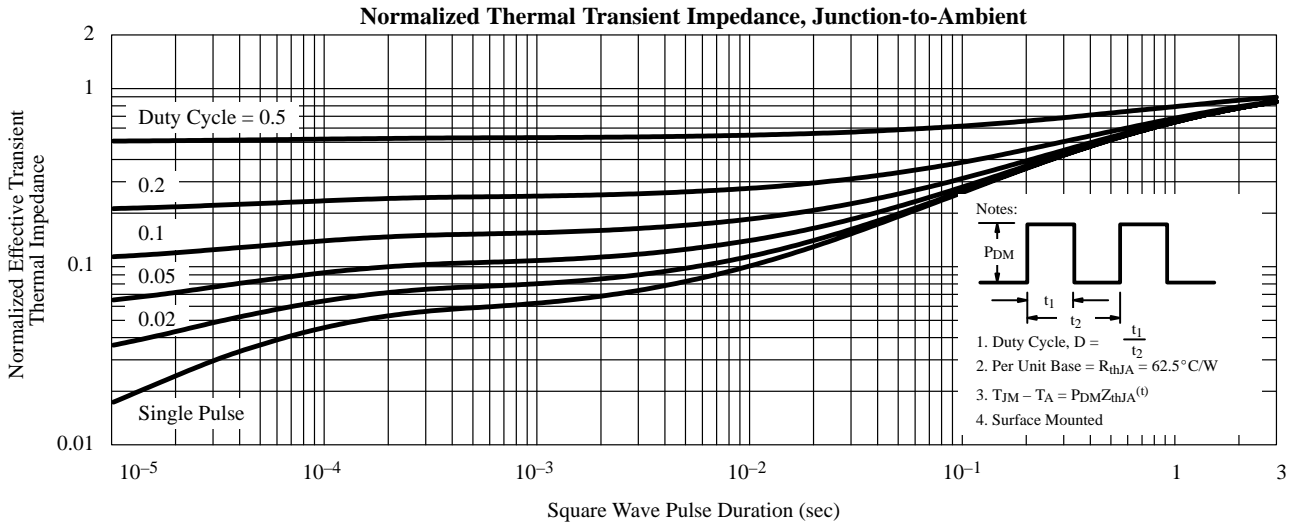
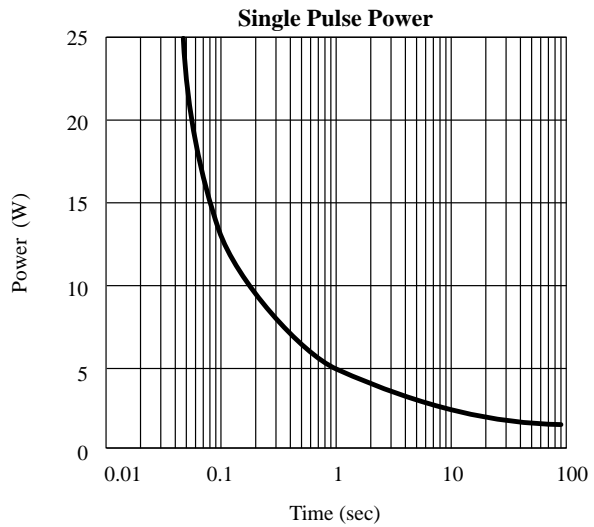
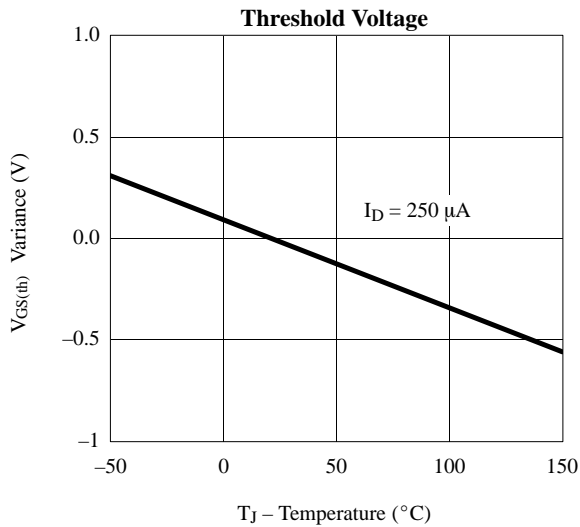
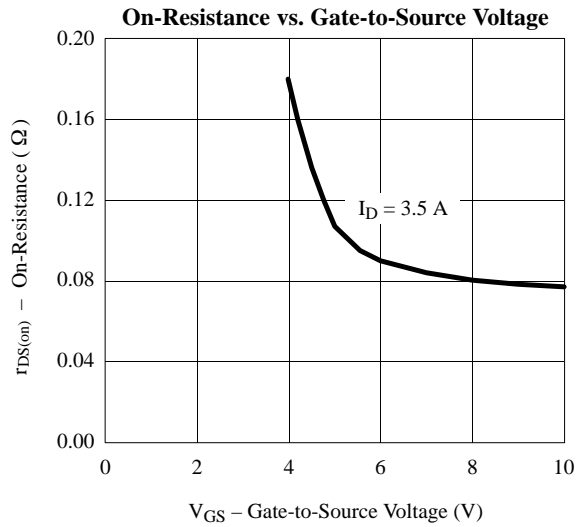
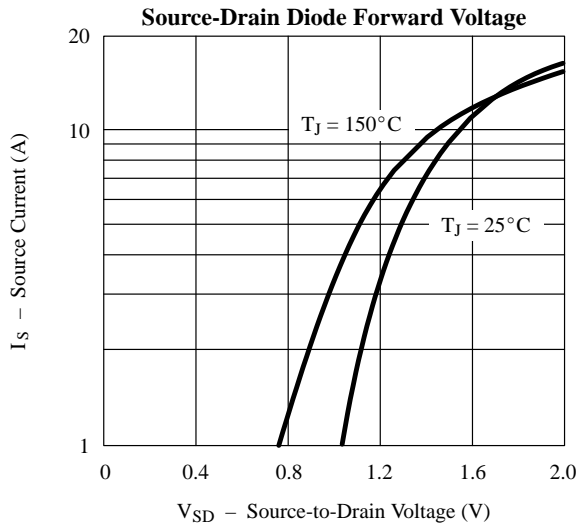
**Typical Characteristics (25°C Unless Otherwise Noted)**

**N-Channel**



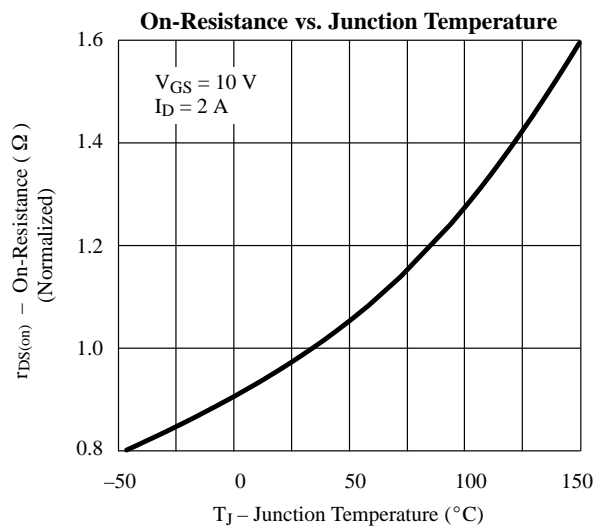
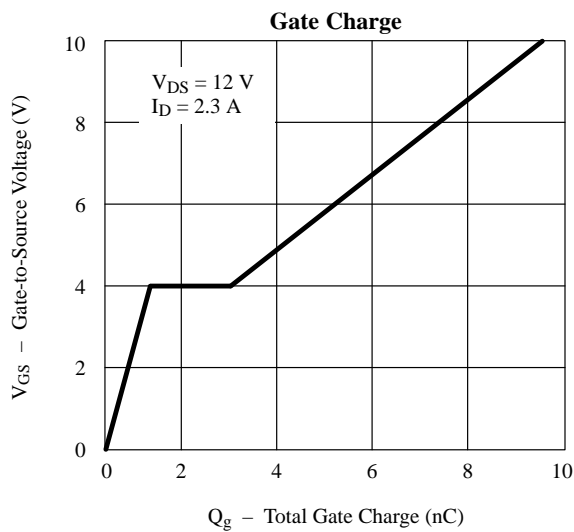
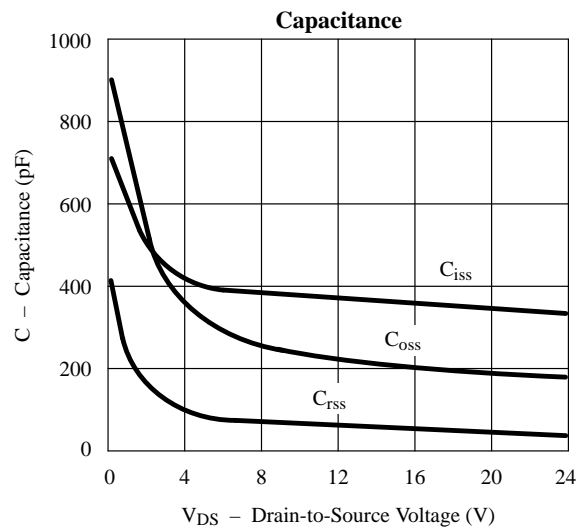
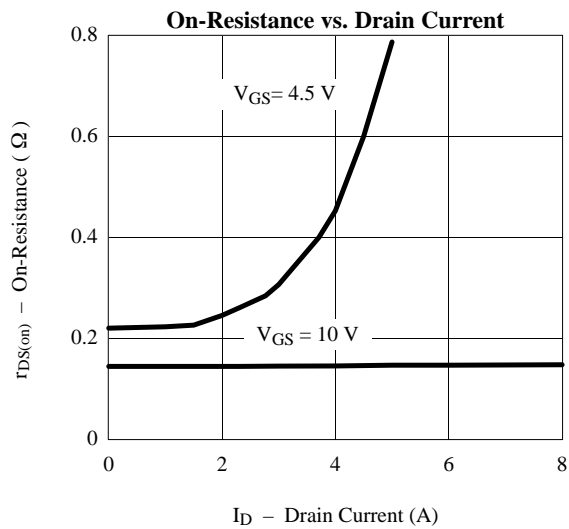
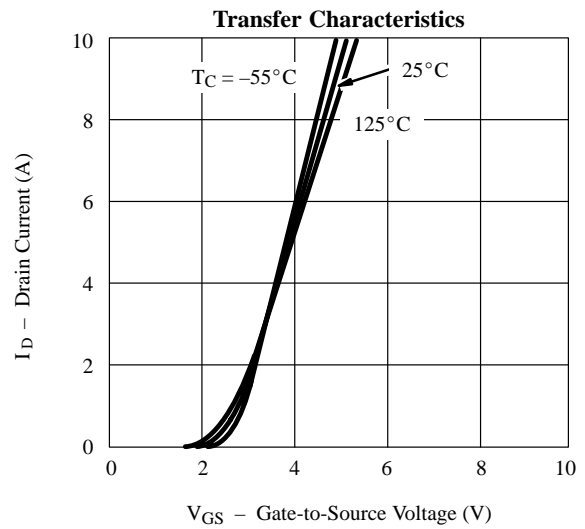
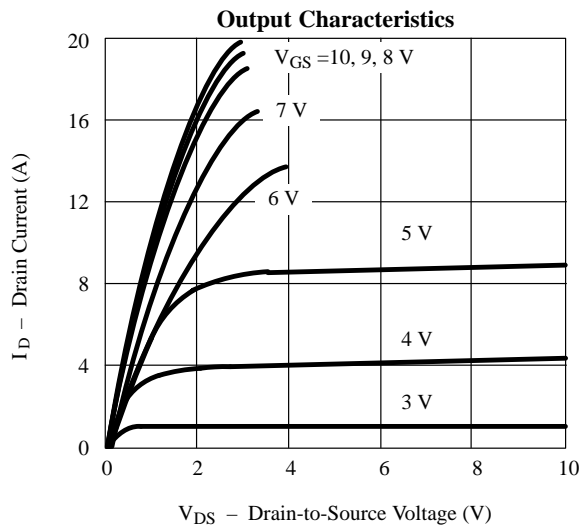
## Typical Characteristics (25°C Unless Otherwise Noted)

## N-Channel



**Typical Characteristics (25°C Unless Otherwise Noted)**

**P-Channel**



## Typical Characteristics (25°C Unless Otherwise Noted)

## P-Channel

